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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/604,067	06/26/2000	Ming-Dou Ker	TSMC2000-004	2697

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EXAMINER
RODRIGUEZ, ISABEL

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 02/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/604,067	KER ET AL.	
	Examiner	Art Unit	
	Isabel Rodriguez	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *21 and 23-28* is/are allowed.

6)☒ Claim(s) *1-11,13,20 and 22* is/are rejected.

7)☒ Claim(s) *12 and 14-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 June 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-9 and 12 are rejected under 35 U.S.C. 102(b) as being anicipated by Ker (IEEE Tyransactions on Electron Devices Vol.46 No. 1)

a) Regarding claim1, Ker discloses an electrostatic discharge (ESD) protection circuit (Fig. 7) that is connected between a first terminal (VSS) and a second terminal (VDD) of an Integrated Circuit (IC), whereby ESD protection circuit comprises: a ESD pulse clamp means for shunting said electrostatic pulse from said IC having a first port that is connected to said first terminal of said IC, a second port that is connected to said second terminal of said IC, and a third port; and an ESD pulse detection means (R, C, Mp, Mn) having a first input port connected to said first terminal of said IC, a second input port connected to said second terminal of said IC, an output port that is connected to said third port of said ESD pulse clamp means, whereby in detecting a presence of said electrostatic pulse said ESD pulse detection means generates a voltage that triggers said ESD pulse clamp means thereby shunting said electrostatic pulse from said IC.

b) Regarding claim 2, Ker discloses that said ESD pulse detection means contains a network comprising a resistive (R) component having a first and a second terminal, a capacitive component (C) having a first and a second terminal, and a voltage inverter.

c) Regarding claim 3, Ker discloses that said voltage inverter comprises a PMOS (Mp) device and a NMOS device (Mn), whereby said voltage inverter contains a first port, a second port, a third port, and a fourth port.

d) Regarding claim 4, Ker discloses that said first port of said voltage inverter is connected to said first terminal of said IC, while said second port of said voltage inverter is connected to said second terminal of said IC. See Fig. 7.

e) Regarding claim 5, Ker discloses that said connections of gate of said PMOS device and of said NMOS device are commonly connected to said third port of said voltage inverter.

f) Regarding claim 6, Ker discloses that said connection of drain and said connection of bulk of said PMOS device are commonly connected to said first port of said voltage inverter.

g) Regarding claim 7, Ker discloses that said connection of source and said connection of bulk of said NMOS device are commonly connected to said second port of said voltage inverter.

h) Regarding claim 8, Ker discloses that said connection of source of said PMOS device and said connection of drain of said NMOS device are commonly connected to said fourth port of said voltage inverter

i) Regarding claim 9, Ker discloses that said capacitive component (C) has a first terminal connected to said first terminal of said IC, said resistive component has a second terminal connected to said second port of said IC, and a second terminal of said capacitive

component and said first terminal of said resistive component are commonly connected to said third port of said voltage inverter.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 10-11 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ker et al. in view of Lien (US 5,086,365)

Ker et al. discloses the circuit of claim 1 wherein said first port of said ESD pulse clamp means comprises a CMOS device and is connected to said first terminal of said IC, said second port of said ESD pulse clamp means is connected to said second terminal of said IC, said third port of said ESD pulse clamp means is connected to said fourth port of said voltage inverter, said connections of bulk and drain of said CMOS device are commonly connected to said first port of said ESD pulse clamp means, said connection of source of said PMOS device is connected to said second port of said ESD pulse clamp means, said connection of gate of said CMOS device is connected to said third port of said ESD pulse clamp means. Ker et al. does not disclose that the MOS device is a PMOS device. Lien shows that a PMOS device is an equivalent structure known in the art by disclosing different circuit configurations for providing protection in which the ESD pulse clamp means are PMOS devices (410) and CMOS (410) devices interchangeably.

Therefore, because these two MOS devices were art-recognized equivalents at the time the invention was made, it would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute a CMOS device with a PMOS device.

5. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ker et al. in view of Mead (Introduction to VLSI systems)

Ker et al. discloses the circuit of claim 2 wherein said capacitive component of said ESD pulse detection means comprises a MOS device having connections of gate electrode, source, drain and bulk, said connections of source, drain and bulk of said PMOS device are commonly connected to said first terminal of said capacitive component, said connection of gate is connected to said second terminal of said capacitive component. Ker et al. does not disclose that such the capacitive component is a PMOS device. Mead discloses the principle behind the use of MOS devices as capacitance. It is inherent that such principles apply to CMOS and PMOS devices as well. It would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the CMOS device for a PMOS device because these two were art-recognized equivalents.

6. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ker et al. in view of Mead in further view of Lien.

The claim discloses the limitations in claims 11 and 13 and is rejected accordingly.

Allowable Subject Matter

7. Claims 12, 14-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. Claims 21 and 23-28 are allowed.

9. The following is a statement of reasons for the indication of allowable subject matter:

The references of record do not teach or suggest the specific connection configurations disclosed in such claims nor would it be obvious to modify those references to include such information.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Isabel Rodriguez whose telephone number is 703-305-4761. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 703-308-3119. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7724 for regular communications and 703-308-7704 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

IR
February 3, 2003

BRIAN SIRCUS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800